## REMARKS

### Claim Rejections 35 U.S.C. § 102 (a)

The Examiner has rejected claims 8, 10-12, 14, and 123-126 under 35 U.S.C. §102 (a) as being anticipated by Matsumoto et al. (U.S. 5,726,479, of record).

Applicants respectfully disagree with the Examiner. Applicants have amended claim 8. An embodiment of Applicants' claimed invention as claimed in claim 8, as amended, is shown in Figure 3I.

Claim 8, as amended, of Applicants' claimed invention, claims a gate electrode, including: a gate layer (320) located over a substrate (300); thin first spacers (330) located adjacent to opposite sides of the gate layer; thick second spacers (340) located adjacent to the thin first spacers, the thin first spacers and the thick second spacers having sidewalls that are parallel to each other along their entire height wherein the gate layer, the thin first spacers, and the thick second spacers have approximately the same height; and a conductive layer (360) located over the gate layer, the conductive layer extending laterally over the thin first spacers but not over sidewalls of the gate layer and not over the thick second spacers. See Figures 3A-3I.

In contrast, the gate electrode of Matsumoto et al. fails to teach the thin first spacers and the thick second spacers having sidewalls that are parallel to each other along their entire height. See Figures 1-3, 5-8, 10, 12, 14-15, 17-19, 21-23.

Thus, Matsumoto et al. fails to teach each and every element of Applicants' claimed invention, as claimed in claim 8, as amended. Consequently, Matsumoto et al. does not anticipate Applicants' claimed invention, as claimed in claim 8, as amended.

Claims 10-12, 14, and 123-126 are dependent on claim 8, as amended. Thus, Yu et al. also fails to teach each and every element of Applicants' claimed invention, as claimed in claims 10-12, 14, and 123-126. Consequently, Matsumoto et al. also does not anticipate Applicants' claimed invention, as claimed in claims 10-12, 14, and 123-126.

In view of the foregoing, Applicants respectfully request the Examiner to withdraw the rejections under 35 U.S.C. §102 (e) to claims 8, 10-12, 14, and 123-126.

**Claim Rejections 35 U.S.C. § 103 (a)**

The Examiner has rejected claims 127 and 128 under 35 U.S.C. §103 (a) as being unpatentable over Matsumoto et al. (U.S. 5,726,479, of record).

Applicants respectfully disagree with the Examiner. Claim 123 is dependent on claim 8. Applicants have amended claim 8. An embodiment of Applicants' claimed invention as claimed in claim 8, as amended, is shown in Figure 3I.

Claim 8, as amended, of Applicants' claimed invention, claims a gate electrode, including: a gate layer (320) located over a substrate (300); thin first spacers (330) located adjacent to opposite sides of the gate layer; thick second spacers (340) located adjacent to the thin first spacers, the thin first spacers and the thick second spacers having sidewalls that are parallel to each other along their entire height wherein the gate layer, the thin first spacers, and the thick second spacers have approximately the same height; and a conductive layer (360) located over the gate layer, the conductive layer extending laterally over the thin first

spacers but not over sidewalls of the gate layer and not over the thick second spacers. See Figures 3A-3I.

In contrast, the gate electrode of Matsumoto et al. fails to teach the thin first spacers and the thick second spacers having sidewalls that are parallel to each other along their entire height. See Figures 1-3, 5-8, 10, 12, 14-15, 17-19, 21-23.

Thus, Matsumoto et al. fails to render Applicants' claimed invention, as claimed in claim 8, as amended, obvious to one of ordinary skill in the art of making semiconductors.

Claims 127 and 128 are dependent on claim 8. Consequently, Matsumoto et al. also fails to render Applicants' claimed invention, as claimed in claims 127 and 128, obvious to one of ordinary skill in the art of making semiconductors.

In view of the foregoing, Applicants respectfully request the Examiner to withdraw the rejections under 35 U.S.C. §103 (a) to claims 127 and 128.

## Conclusion

Applicants believe that all claims pending, including claims 8, 10-12, 14, and 123-128, are now in condition for allowance so such action is earnestly solicited at the earliest possible date.

Pursuant to 37 C.F.R. 1.136 (a) (3), Applicants hereby request and authorize the U.S. Patent and Trademark Office to treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time.

Should there be any additional charge or fee, including a Request for Continued Examination, an extension of time fee, or other fees under 37 C.F.R. 1.16 and 1.17, please charge Deposit Account No. 50-0221.

If a telephone interview would in any way expedite the prosecution of this application, the Examiner is invited to contact the undersigned at (408) 720-8300.

Respectfully submitted,
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